1. SPECIFICATIONS

The general description of the card is FADICLOCK parallel to the description of the integrated circuit DS3232SN that supports a temperature range of -40 º C to +85 ° C. I2C/SMBus-400kHz By accessing the card that hosts the full FADICLOCK DS3232SN RTC clock that has a valid calendar to 2099, 2-day alarms monthly or weekly day, a block of 236 bytes SRAM, a wave generator programmable square 1Hz, 1024kHz, 4096kHz or 8192kHz, a square wave generator fixed 32kHz, a digital temperature sensor with a record setting compensation for aging and a bidirectional reset system.

The DS3232 supply voltage is set between 2'3v and 5'5v, this allows the card to operate indiscriminately FADIBUS 3'3v or 5v. The load current is greater than 5v to 3'3v. Consumption increases when operating with the I2C bus using the 32kHz output, using the alarm output or programmable wave or while making a temperature conversion. A 3'3v consumed from 120µA if idle (keeping the RTC SRAM i) up to 500 uA. A 5v consume between 160 uA and 600 uA.

Alternatively it can be powered by a battery with the same voltage range, the lower the supply voltage operates the DS3232 with battery but some features can be enabled or desactivadasen introduced depending on the configuration. DS3232 widely used to program the operation mode that should have in case of failure of the supply voltage. The power failure occurs when the voltage Vcc drops below the Vbat.

The DS3232SN unlike other RTC has an internal oscillator that maintains offset precision of ± 2min per year if it respects the range of temperature range -40 º C to +85 ° C.

The return address on the I2C bus is fixed and responds to address $ D0-$ D1.

2. INTERNAL REGISTERS

The bytes and nibbles of the internal registers using the BCD system, all records can be read and some of the bits of the bytes or bits operate as control configurators.

The byte-time ($ 02), bit 6 set the time as 12/24horas:

Bit6 = 1 sets the RTC to 12, then bit (5) HIGH indicates that it is PM, LOW indicates AM. The bit (4) indicates the tens of hours.

Bit6 = 0 sets the RTC to 24h, then the bit (5) and bit (4) numbered tens of hours.

The byte-month ($ 05), bit 7 is a flag end of a century, bit (7) is set to HIGH indicates that there has been a turn of the century.

Internal adress	Bit 7		Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function	Range
$00	0		10 seconds			seconds				Seconds	00-59
$01	0		10 minutes			minutes				Minutes	00-59
$02	0		0 ->24h	10 hour		hour				Hours	00-23
			1 -> 12h	0.-AM 1.-PM	10 hour						1-12 $\overline{\text{AM}}$/PM
$03	0		0	0	0	0	day			Day	1-7
$04	0		0	10 Date		date				Date	00-31
$05	century		0	0	10 month	month				Month/Century	01-12 F siglo
$06	10 year					year				Year	00-99
$07	A1M1	Forma disparo alarma_1	10 seconds			seconds				A1 seconds	00-59
$08	A1M2		10 minutes			minutes				A1 Minutes	00-59
$09	A1M3		0 ->24h	10 hour		hour				A1 Hour	00-23
			1 -> 12h	0.-AM 1.-PM	10 hour						1-12 $\overline{\text{AM}}$/PM
$0A	A1M4		1 day	X	X	Code day				A1 Day	1-7
			0 date	10 date		date				A1 Date	01-31
$0B	A2M2	Forma disparo alarma_2	10 minutes			minuts				A2 Minutes	00-59
$0C	A2M3		0 ->24h	10 hour		hour				A2 Hour	00-23
			1 -> 12h	0.-AM 1.-PM	10 hour						1-12 $\overline{\text{AM}}$/PM
$0D	A2M4		1 day	X	X	Code day				A2 Day	1-7
			0 date	10 date		date				A2 Date	01-31
$0E	$\overline{EOSC}$		$BBSQW$	$CONV$	$RS2$	$RS1$	$NTCN$	$A2IE$	$A1IE$	Control	
$0F	OSF		$BB32kHZ$	$CRATE1$	$CRATE0$	$EN32kHZ$	BSY	$A2F$	$A1F$	Control/Status	
$10	$SIGN$		$DATA\_2^6$	$DATA\_2^5$	$DATA\_2^4$	$DATA\_2^3$	$DATA\_2^2$	$DATA\_2^1$	$DATA\_2^0$	Aging offset	Comp 2
$11	$SIGN$		$DATA\_2^6$	$DATA\_2^5$	$DATA\_2^4$	$DATA\_2^3$	$DATA\_2^2$	$DATA\_2^1$	$DATA\_2^0$	MSB Temperature	Comp 2
$12	$DATA\_2^{-1}$		$DATA\_2^{-2}$	0	0	0	0	0	0	LSB Temperature	
$13	0		0	0	0	0	0	0	0	Reserved	Reser.
$14-$FF	$DATA\_2^7$		$DATA\_2^6$	$DATA\_2^5$	$DATA\_2^4$	$DATA\_2^3$	$DATA\_2^2$	$DATA\_2^1$	$DATA\_2^0$	SRAM	00-FF

Form trigger the alarm 1.

$DY/\overline{DT}$	ALARM_1 REGISTER MASK				
	A1M4	A1M3	A1M2	A1M1	
	1	1	1	1	Only once, on a date / hour / minute / second accurate.
	1	1	1	0	Retriggerable per second.
	1	1	0	0	Retriggerable minutes and seconds.
	1	0	0	0	Retriggerable hours, minutes and seconds.
0	0	0	0	0	Retriggerable daily-weekly, hours, minutes and seconds.
1	0	0	0	0	Retriggerable daily-weekly, hours, minutes and seconds.

Form trigger the alarm 2.

$DY/\overline{DT}$	ALARM_2 REGISTER MASK			
	A2M4	A2M3	A2M2	
	1	1	1	Sólo una vez, en fecha/hora/minuto y 00 segundos exacto.
	1	1	0	Retriggerable minutes.
	1	0	0	Retriggerable hours, minutes.
0	0	0	0	Retriggerable date, hours, minutes.
1	0	0	0	Retriggerable day, hours, minutes.

The day of the week and day of the month have separate records when it ends one day (23h 59m 59s 11h 59m 59s or PM) concurrently increases on monthly and weekly day.

The alarm mode monthly day registration only takes into account the day (ALM1: $ 0A or ALM2: $ 0D) which can be monthly or weekly and monthly day compared to the RTC ($ 04).

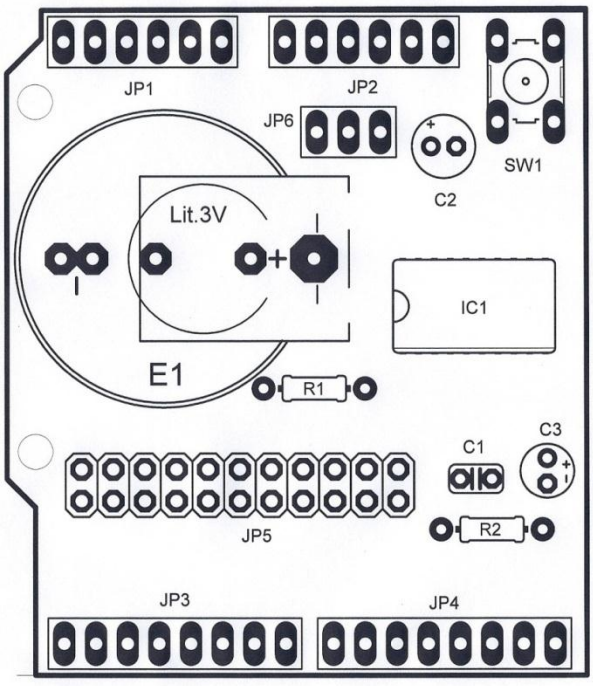
Likewise if an alarm is set at weekly day, compares his record day (ALM1: $ 0A or ALM2: $ 0D) with the weekly day of RTC ($ 03).

3. LIST OF COMPONENTS

$1PCB_1$	1015 014	PCB FADICLOCK.
IC_1	1010 506	DS 3232SN
SW_1	1003 000	Push button.

R_1- R_2	1002 472	Resistance 4.7KΩ 1/4w.
C_1	1002 472	ceramic capacitor 100nF 50v.
C_2	1002 472	electrolytic capacitor 22µF 16v.
C_3	1002 472	If operating without battery, we recommend placing a capacitor.
JP_1-JP_2	1000 501	Pair of 6 and 8 tracks.
JP_3-JP_4	1000 501	Pair of 6 and 8 tracks.
JP_5	1004 222	Connector 22 pins terminals bent.
JP_6	1004 103	Connector 3 pins terminales straight.
E_1	1003 001	Battery holder 20mm. CR20xx
S_1	1003 001	Red jumper.
S_2- S_6	1003 002	Blue jumper.

4. MAP OF COMPONENTS



5. EXTERNAL SETTINGS

5.1. Card power

The card can be powered FADIBUS or 3.3 v 5v. Given that the card provides PICAXE BASE SHIELD 5V or 3.3 V with a current of up 0'5A between both sources, however ARDUINO explicitly provides ONE-0'5A 5v and 3.3 v-0'1A. In both cases it is preferable to use 5v microcontrollers and feed FADIBUS with the primary power supply (5V). In any case, FADICLOCK fits both voltages are selected with a red jumper S1.

5.2. I2C slave adress

FADICLOCK responds only to the address $D0-$D1.

5.3. Activation of the interrupt.

If you configure the DS3232 RTC to generate alarms, there is an interruption by LOW through the pin SQW / INT whenever ALARMA_2 ALARMA_1 or reach the point in time schedule.

If configured as the RTC DS3232 programmable waveform generator, a signal is produced synchronously by the pin SQW / INT whose frequency is defined by internal bits RS1 and RS2.

5.4. Resistance pullup SQW/INT.

Output interruption has two states: LOW level (interruption) and high impedance (no interruption), to obtain a HIGH level output is connected interruption SQW / INT to Vcc through the resistor R1.

The output SQW / INT always requires an external pullup resistor R1 in either the same card or another. The card can be a function FADICLOCK O-logic with other cards to enable interrupts via the same input, the only requirement is that one must be active pullup resistor. In this case using a bridge card RS is chosen to provide the only operational pullup resistor.

5.5. Routing interrupt to the microcontroller.

If you configure the DS3232 RTC to generate alarms, pin SQW / INT channels or internal events and interruptions ALARMA_1 ALARMA_2. Using a blue bridge, the card may direct that interruption FADICLOCK was bypassing the microcontroller B.0, B.1, B.2, or C.6 C.7 ports B and C respectively.

If you configure the DS3232 RTC as a programmable waveform generator, the pin SQW / INT wave channels programmed into the internal bits RS2 and RS1. Using a blue bridge, the card can route the signal FADICLOCK wave generator programmable microcontroller made bypassing B.0, B.1, B.2, C.6 C.7 or ports B and C respectively.

5.6. Routing interrupt wave signal 32khz(2^{15}=32768Hz)

If the generator of 32kHz is enabled (EN32kHZ), can be routed to pins or C.4 C.5. The card connector JP5 FADICLOCK have to insert a bridge in the area and route 32KHZ signal to the pin or C.4 C.5.

Since it is a push-pull output of 1mA does not require auxiliary heaters.

5.7. Routing interrupt reset signal.

The reset pin is a pin DS3232SM input and output simultaneously. Internally has a resistance of 50kΩ pullup addition FADICLOCK card inserted in a parallel pullup resistor R_1 4k7Ω; itself does not suit can be detached.

The DS3232 initializes internal reset cycle when applying a LOW level.

When the supply voltage Vcc is located below the battery voltage then acts as an output RESET pin putting the LOW level.

Using a jumper can be routed to the reset signal inputs or C.1 C.0

FADICLOCK card has a reset button to reset the card microcontroller easily. Placing a jumper on the left end of JP5 connector, labeled RESET can be connected to the reset circuit microcontorlador the reset circuit DS3232SN.

6. INTERNAL CONFIGURATION

6.1. Alarms

The pin INT / SQW is shared with 2 internal devices. To implement this pin as output alarm interrupt, we first need to put the control bit_2 SQW / INT HIGH.

Second, to avoid generating an interrupt during configuration, you must disable the alarms in the control register, making low and A2IE A1IE bits.

Thirdly you must type in the internal functional registers $ 07 - $ 0D considering their masks A2M1 A1M1-4 and-3.

Fourth to acknowledge the alarm that exploded must clear the flags and alarma_2 alarma_1, bit_1 bit_0 and the status register, A1F and A2F respectively.

And finally enable alarms HIGH putting the bits 1 and 2 of control register, and A2IE A1IE respectively.

If no backup battery, connecting the DS3232SN (power-up) will occur following

 INTCN HIGH INT / SQW is configured to alarm interrupts.

A1IE, A2IE AT Alarms are disabled on the first connection.

6.2. PROGRAMMABLE WAVEFORM GENERATOR SQW.

Since the pin INT / SQW is shared. To implement this pin as an output square wave generator, you can include the control bit_2 SQW / INT to LOW level.

The square wave generator 4 has preprogrammed fixed frequencies:

RS2	RS1	Output frequency SQW
0	0	2^0 1 Hz
0	1	2^{10} 1024 Hz
1	0	2^{12} 4096 Hz
1	1	2^{13} 8192 Hz

In the control register bits 4 and 5, RS2 and RS1 respectively constitute one of the four frequencies.

When DS3232SN connects for the first time BBSQW bit_6 control register is LOW. That means that if the battery voltage is higher than Vcc Vbackup then the waveform generator will be off and the pin INT / SQW no signal. If you want to continue generating signal INT / SQW should be a bit HIGH _6 BBSQW that consuming battery power will continue to oscillate.

If the battery voltage Vcc is higher than the battery voltage will always be Vbackup output signal of the signal presciendiendo BBSQW, which serves only to when it falls Vcc.

6.3. SIGNAL DE 32768KHZ

32kHz output is a square wave generator 32768Hz fixed (215 Hz) that internally has an output stage push-pull reaching 1mA supply current.

To enable this to be the bit_3 generator control register / status EN32kHZ to HIGH.

If you want to continue generating this signal when Vbat> Vcc then you have to put HIGH bit_6 register the control / status. If this bit_6 BB32KHZ = 0 then there is a failure in the supply voltage Vcc 32kHz output pin will remain low.

6.4. TEMPERATURE CONVERSION

The DS3232SN has a temperature sensor internally compensated by registration. It has a resolution of 0.25 ° C and a range of -40 ° C to +85 ° C. Reading the record function $ 11 you can access the entire $ 12 is accessed to the decimal. The temperature is encoded in 2's complement, the most significant bit of the integer part of $ 11 is the sign (0. - Positive, 1. - Negative), the 7 remaining bits form the magnitude of the temperature.

Temperature conversions are performed after startup and thereafter at a rate of bit_5 i configured in the registry bit_6 control / status, and CRATE0 CRATE1 respectively:

CRATE1	CRATE0	Cadence conversion de temperature
0	0	64 seconds
0	1	128 seconds
1	0	256 seconds
1	1	512 seconds

Additional functionality is widely used in the conversion of temperature is the control register bit_5 CONV. Under normal circumstances / LOW level is stable at a HIGH level put it through a script, is forced to perform a temperature conversion with immediate effect. At that time the flag BSY bit_2 located in the control register / status is set to HIGH level indicating that the temperature conversion is in progress.

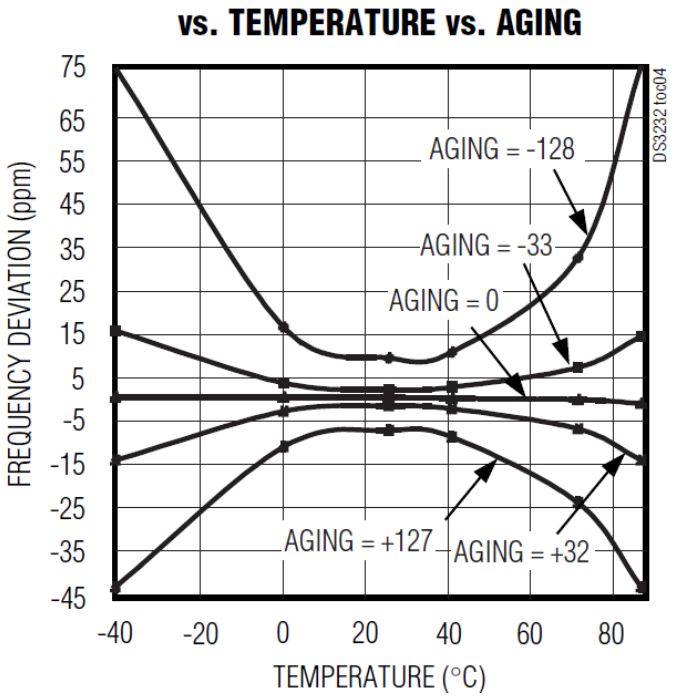
When the conversion is completed the BSY flag is put back to LOW level to indicate that the temperature converter is made free to order a new one. The result of the previous conversion is stored in the log function of temperature $ 11 - $ 12.

6.5. CORRECTION OF TEMPERATURE CONVERSION

Internally there is a capacitor array connected to the crystal oscillator. Sometimes the DS3232SN aging or due to a temperature far from the normal 25 ° C causes the loss of linearity and accuracy. To correct this effect exists AGING registration OFFSET adds or subtracts capacitance to the oscillator, ie internal capacitors connected or disconnected.

The effect is that it causes a change in the oscillation frequency of 32kHz, well used to correct the frequency of oscillation at its real value. Registration aging is implemented in 2's complement. A positive value in the register Aging ($ 10) adds capacity and causes a decrease in the frequency of internal oscillation, contrary to a negative value extracted capacity and increases the frequency of oscillation. At pin can be monitored 32kHz frequency changes. To calculate the value to be written must use the following chart provided by

http://www.maxim-ic.com :



6.6. INTERNAL OSCILLATOR

Sometimes the 32kHz internal oscillator can not be launched or is temporarily unavailable. It also indicates that some time has been without scrolling. This happens:

A. - During the startup.

2. - Because Vbackup or Vcc voltages applied are inadequate.

3. - $(EOSC)^{-}$ = 0 but is powered by battery.

4. - When external influences act and indisponen (noise ...).

For state forThe internal oscillator bit_7 reads the control register / status. A HIGH level indicates alarm, which is stopped or was stopped. This bit will remain in high state until you write a LOW level.

If the first startup is caused by a battery (Vcc = 0 and Vbackup = E) then, to save power the internal oscillator will not start until:

A. - Vcc> Vbackup

2. - The enter a valid $ $ D0-D1 on the I2C bus.

6.7. Battery.

Backup battery acts automatically whenever the supply voltage Vcc is generally lower than the battery voltage.

There are a control register bits that modify the behavior of the oscillator to a drop in Vcc.

The control register bit_7 used to stop the internal oscillator as the DS3232SN is powered by Vbackup. Put a HIGH level at $(EOSC)^{-}$ commissioning prevents internal oscillator and thus saving battery energy. By default $(EOSC)^{-}$ is LOW and there is a battery, the oscillator continues to operate in a fall of Vcc.

The control register bit_6 BBSQW default is LOW. In this situation with a drop of Vcc the programmable square wave generator stops working and pin INT / SQW remains in high impedance state. In this way helps to save battery energy.

If BBSQW is HIGH, whether that is a drop in Vcc, then the programmable square wave generator will continue to operate on battery power.

7. Interface I^2C

For more information refer to http://www.maxim-ic.com

The bus will always be accessible if Vcc or Vbackup levels are valid.

Sometimes if the microcontroller is reset or loses power while you are communicating via the I2C can stay DS3232SN sync. You can restore it when the microcontroller has recovered Vcc and detect the lack of communication. The method involves swinging SCL to note that the SDA puts DS3232SN HIGH level at that time while SCL is HIGH, the microcontroller sets SDA to LOW level. Another way to restore DS3232SN is to keep a long time SCL low.